a receiver for receiving signals on the single communications channel;

processing means for indicating whether the UART is operating in a full duplex mode of operation; and

receiver control circuitry for disabling [and enabling] the receiver in response to the indication of a full duplex mode of operation by the processing means.

C1

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~~13~~. (Amended) The UART of Claim ~~12~~ wherein the receiver control circuitry further disables [and enables] the receiver in response to the signal indicating data for transmission in the means for storing.

C2

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~~15~~. (Amended) The UART of Claim ~~14~~ wherein the receiver control circuitry disables [and enables] the receiver in response to signals indicating data stored within the data store and the FIFO.

C3

6 1 17
~~17~~. (Amended) The UART of Claim ~~16~~ wherein the receiver control circuitry further [enables and] disables the receiver in response to the indication of whether the receiver enable flag has been set.

E

C4

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~~18~~. (Amended) An apparatus for providing single channel communications, comprising:

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a transmitter for transmitting signals on a single communications channel;

a receiver for receiving signals on the single communications channel;

processing means for generating an indication of at [lease] least one of whether the apparatus is in a full-duplex mode and whether [the] a receiver enable flag is set;

means for storing data to be transmitted by the transmitter, the means for storing generating an indication when data for transmission is contained therein; and

receiver control circuitry for disabling [and enabling] the receiver in response to at least one of the indications of whether the apparatus is in a full duplex mode, the indication of whether the receiver enable flag is set and the indication of whether the means for storing contains data for transmission.

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21. (Amended) A control circuit for a UART, comprising:

means for receiving at least one of a first indicator of whether the UART operates in a full-duplex mode, a second indicator of whether a receiver flag is set, a third indicator of whether data for transmission is stored; and

control circuitry for completely disabling a receiver responsive to at least one of the first, second and third indicators.

REMARKS

In response to the Office Action dated October 16, 1997, the Applicant has amended Claims 11, 13, 15, 17, 18 and 21. Thus, Claims 11-21 are now pending in the application. Reconsideration of the claims, as amended, is respectfully requested.

The Examiner rejected Claims 11-21 under 35 U.S.C. § 102b as being anticipated by Hamilton. Applicant respectfully traverses. In particular, the Examiner stated that the Hamilton reference illustrated a processing means for indicating whether a UART was operating in a full duplex mode of operation at column 27, lines 10-20. The Applicant respectfully submits that the cited portion of the reference merely discloses that the digital encryption device has an input/output port capable of full duplex, serial functionality. The reference does not disclose a processing means that provides an indication of whether the UART is operating in a full duplex mode of operation. In fact, there is no indication in the cited reference that the input port is capable of full and half duplex modes of operation. Thus, no means for indicating the mode is needed.

The Examiner also states that the Hamilton reference discloses at Column 52, lines 42-62, receiver control circuitry for disabling and enabling the receiver in response to an indication of the full